Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.020”**

**ANODE**

**.015 x .015”**

**.020”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .015” X .015”**

**Backside Potential: CATHODE**

**Mask Ref: ZMB**

**APPROVED BY: DK DIE SIZE .020” X .020” DATE: 5/19/22**

**MFG: ALLEGRO / SPRAGUE THICKNESS .008” P/N: THZ012A05**

**DG 10.1.2**

#### Rev B, 7/19/02